What is claimed is:

1. An emulation logic board, comprising:

at least one integrated circuit having reconfigurable logic resources; and

on-board processing resources, in communication with the at least one integrated circuit, operable to configure the integrated circuit.

2. The emulation logic board of claim 1, further comprising a plurality of integrated circuits, each having reconfigurable logic resources, the on-board processing resources being operable to configure each of the reconfigurable logic resources of each of the integrated circuits.

3. The emulation logic board of claim 1, wherein the integrated circuit further includes reconfigurable input/output resources, the on-board processing resources being further operable to configure the reconfigurable input/output resources.

4. The emulation logic board of claim 1, wherein the on-board processing resources comprise:

memory having stored therein programming instructions for configuring the integrated circuit; and

a processor coupled to the memory to execute the programming instructions.

5. The emulation logic board of claim 1, further comprising reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, wherein the on-board processing resources are operative to configure the reconfigurable interconnects.

6. The emulation logic board of claim 1, wherein the on-board processing resources are operable to configure the integrated circuit in response to external commands.

7. The emulation logic board of claim 6, wherein the external commands comprise a data packet.

8. The emulation logic board of claim 7, wherein the data packet comprises:

a packet header;

a command field following the packet header;

a parameter field following the command field; and

an end-of-packet marker following the parameter field.

9. The emulation logic board of claim 1, wherein the integrated circuit comprises on-chip data processing resources operative to assist the on-board processing resources to perform the configuration of the integrated circuit.

10. The emulation logic board of claim 1, wherein the on-board processing resources are further operable to perform emulation functions on a configured integrated circuit.

11. The emulation logic board of claim 10, wherein the emulation functions comprise generating testing stimuli and applying testing stimuli to an appropriate pin of the at least one integrated circuit.

12. The emulation logic board of claim 10, where the emulation functions comprise:

locally determining emulation state elements of a design being emulated;

reading state data of the emulation state elements to detect occurrence of certain events; and

reporting the occurrence of the events upon detection.

13. The emulation logic board of claim 10 wherein the on-board processing resources are operable to perform emulation functions responsive to external commands.

14. In an emulation logic board comprising at least one integrated circuit, having reconfigurable logic resources and on-board processing resources, in communication with the at least one integrated circuit, a method of configuring the emulation logic board comprising:

receiving, by the on-board processing resources, a command for configuring the logic board; and

configuring the emulation logic board in accordance with the command received by the on-board processing resources.

15. The method of claim 14, wherein configuring the emulation logic board in accordance with the external command comprises:

locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one integrated circuit; and

applying the locally generated configuration signal to the integrated circuit.

16. The method of claim 14, wherein the emulation logic board further includes reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, and the on-board resources are operative to configure the reconfigurable interconnects, and wherein configuring the emulation board in accordance with the command comprises:

locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one of the reconfigurable interconnects; and

applying the locally generated configuration signal to the at least one reconfigurable interconnect.

17. The method of claim 14, wherein the integrated circuit further comprises on-chip processing resources, configuring the integrated circuit is at least partially performed in conjunction with on-chip data processing resources.

18. An emulation system comprising:

a workstation having electronic design automation (EDA) software to partition an integrated circuit (IC) design into a plurality of partitions; and

at least one emulation logic board in communication with the workstation, comprising:

at least one integrated circuit having reconfigurable logic resources, and on-board processing resources, in communication with the at least one integrated circuit and operable to configure the integrated circuit in response to commands from the EDA software of the workstation.

19. The emulation system of claim 18, comprising a plurality of emulation logic boards.

20. The emulation system of claim 18 wherein the emulation logic board further comprises reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, wherein the on-board resources are operative to configure the reconfigurable interconnects.

21. The emulation system as set forth in claim 18, wherein the on-board processing resources are further operable to perform emulation functions on a configured integrated circuit in response to commands from the EDA software of the workstation.

22. An emulation apparatus comprising:

a plurality of collections of reconfigurable logic resources,

a plurality of collections of reconfigurable I/O resources; and

a plurality of groups of data processing resources correspondingly coupled to the collections of reconfigurable logic and I/O resources to correspondingly and distributively generate configuration signals to configure selected ones of reconfigurable logic and I/O resources to emulate circuit elements of corresponding partitions of an IC design.

23. The emulation apparatus as set forth in claim 22, wherein at least one group of the data processing resources comprises memory having stored therein programming instructions for configuring the collections of reconfigurable logic and I/O resources; and a processor coupled to the memory to execute the programming instructions.

24. An integrated circuit comprising:

a plurality of reconfigurable logic resources;

a plurality of reconfigurable I/O resources; and

on-chip data processing resources, coupled to the reconfigurable logic and I/O resources, operative to configure the reconfigurable logic and I/O resources.

25. The emulation integrated circuit of claim 24, wherein the on-chip processing resources configure selected ones of the reconfigurable logic resources of the integrated circuit.

26. The emulation integrated circuit of claim 24, wherein the on-chip processing resources configure selected ones of the reconfigurable I/O resources of the integrated circuit.

27. The emulation integrated circuit of claim 24, wherein the on-chip processing resources are operable to configure the integrated circuit in response to external commands.

28. The emulation integrated circuit of claim 24, wherein the on-chip processing resources are further operable to perform emulation functions on a configured integrated circuit.

29. In an integrated circuit comprising a plurality of reconfigurable logic resources, a plurality of reconfigurable I/O resources, and on-chip data processing resources, coupled to the reconfigurable logic and I/O resources, operative to configure the reconfigurable logic and I/O resources, a method of operation comprising:

receiving, by the on-chip processing resources, an external command for configuring the integrated circuit; and

configuring the reconfigurable logic and I/O resources in accordance with the external command received by the on-chip processing resources.

30. The method of claim 29 wherein configuring the reconfigurable logic and I/O resources in accordance with the external command comprises:

locally generating on the integrated circuit, by the on-chip processing resources, a configuration signal to configure the at least one of the reconfigurable logic and I/O resources; and

applying the locally generated configuration signal to the at least one of the reconfigurable logic and I/O resources.

31. An emulation logic board, comprising:

at least one integrated circuit having reconfigurable logic resources; and

on-board processing resources, in communication with the at least one integrated circuit, operable to receive a configuration command and generate a configuration signal, in response to the configuration command, to configure the integrated circuit.

32. An emulation logic board, comprising:

at least one integrated circuit having reconfigurable logic resources; and

on-board processing resources, in communication with the at least one integrated circuit, operable to receive a first set of configuration commands and translate the first set of commands into a second set of configuration commands different from the first set.

33. A method comprising steps of:

receiving at an emulation logic board a first set of configuration commands associated with a design;

generating locally at the emulation logic board a second set of configuration commands based on the first set of configuration commands; and

configuring an emulation integrated circuit to map at least the portion of the design in accordance with the second set of configuration commands.